

**SEMICONDUCTOR MEMORY HAVING SENSE AMPLIFIER
ARCHITECTURE**

ABSTRACT OF THE DISCLOSURE

The semiconductor memory device includes a plurality of first data sense amplifiers and a plurality of second data sense amplifiers. Each first data sense amplifier being a voltage sense amplifier, and each first data sense amplifier associated with data lines of a first type, which lead from bit line sense amplifiers. Each second data sense amplifier including a current sense amplifier and a voltage sense amplifier, and each second data sense amplifier associated with data lines of a second type, which lead from bit line sense amplifiers.

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